Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N. CP1**
2. **K1**
3. **J1**
4. **N. SD1**
5. **Q1**
6. **N. Q1**
7. **N. Q2**
8. **GND**
9. **Q2**
10. **N. SD2**
11. **J2**
12. **K2**
13. **N. CP2**
14. **N. CD2**
15. **N. CD1**
16. **VCC**

**.050”**

**2 1 16 15**

**14**

**13**

**12**

**11**

**10**

**LS**

**112A**

**DIE ID**

**3**

**4**

**5**

**.048”**

**6 7 8 9**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: LS112A**

**APPROVED BY: DK DIE SIZE .048” X .050” DATE: 7/8/19**

**MFG: MOTOROLA THICKNESS .020” P/N: 54LS112A**

**DG 10.1.2**

#### Rev B, 7/19/02